



IN THE CLAIMS:

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TECHNOLOGY CENT.

1. (currently amended) A DRAM cell array which comprises:

a plurality of memory cells which are arranged in rows and columns, each memory cell including a deep trench region having a vertical MOSFET and an underlying capacitor formed therein that are in electrical contact to each other through at least one buried-strap outdiffusion region which is present within a portion of a wall of each deep trench; and,

each memory cell having a deep trench conductor forming an electrode of said underlying capacitor and a collar oxide region formed in a portion of the deep trench;

the collar oxide region formed on a remaining wall portion of each deep trench not containing

figs. 2(a) - 2(h) said buried-strap outdiffusion region for electrically isolating a body region ~~contact~~ from said underlying capacitor; and

a trench top oxide (TTO) layer formed on a horizontal surface of the DRAM cell array for isolating the deep trench conductor forming an electrode of said underlying capacitor and said buried-strap outdiffusion region from a gate conductor region;

an underlying nitride layer formed immediately adjacent to and contacting a top of said deep trench conductor between the a top of said deep trench conductor and said buried-strap outdiffusion region and underlying said TTO layer to eliminate a possibility of TTO layer dielectric breakdown between said gate conductor region and said electrode of said underlying capacitor.

2. (cancelled)

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fig. 3

3. (previously amended) The DRAM cell array of Claim 1, further including [a sacrificial oxide layer formed underneath said nitride layer to further eliminate a possibility of TTO layer dielectric breakdown between the gate conductor region and said deep trench conductor]

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cont.

4. (previously amended) The DRAM cell array of Claim 1, wherein said nitride layer is deposited to a thickness ranging from 1.0 nm – 10.0 nm.

5. (previously amended) The DRAM cell array of Claim 1, wherein each said vertical MOSFET includes gate dielectrics formed on inner surfaces of said sidewalls of each said deep trench.

6-15 (withdrawn)

16. (new) The DRAM cell array of claim 1, wherein the underlying nitride layer is formed only under and on the side of the TTO layer.
